REMARKS/ARGUMENTS

Claims 1-30 are pending in this application. Claims 17 and 28-30 have been amended to comply with the Examiner's objections to claim dependencies. It is respectfully submitted that no new matter has been added.

The Abstract of the disclosure was objected to because of its content and format. The Abstract has been amended to comply with the Examiner's objection. It is respectfully submitted that no new matter has been added.

Claims 1, 3-9, 14, 16-22, and 27 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,748,684 to Clifton Sanchez ("Sanchez"). Claims 10-13, 23-26, and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sanchez as applied to claims 1-9, 14-22, and 27-28, and further in view of U.S. Patent No. US 2002/0120882 A1 to Sarangi et al. Claims 2, 15, and 28, are objected to as being dependent upon a rejected base claim.

Claim Rejections under 35 U.S.C. §102(b)

Independent claims 1, 14 and 27 were rejected under 35 U.S.C. §102(b) as anticipated by Sanchez. Sanchez discloses circuitry and a method for re-synchronizing a synchronous bi-directional serial communication link between a controller and a peripheral. To resynchronize, a series of bits are set at a first logic level by the controller. The series of bits is long enough to ensure that the peripheral will decode a command word in which all of the bits are at the first logic level. The peripheral, upon decoding the command word, resets the synchronization circuitry within the peripheral. The controller then sends a single bit of the opposite logic state followed by serial data. The peripheral releases the synchronization circuitry from its reset condition upon receipt of the bit with the opposite logic state. The peripheral then begins to

decode the serial data in synchronization with the controller. (*See* Abstract).

These rejections are traversed, in part, because the cited reference fails to teach or suggest features of the presently claimed invention for communicating between a device and a controller. For example, Sanchez fails to teach or suggest verifying the timing reference through analysis of the guard clock signal in relation to the clock signal, as recited in claims 1, 14, and 27.

Sanchez does not teach a system or method for verifying a timing reference through analysis of a guard signal in relation to a clock signal. Instead, Sanchez teaches the use of the clock signal to clock data into the serial data in pin (SDI) and out of the serial data out pin (SDO) without verifying the accuracy of the clock reception. The Examiner claims the data ready bar pin (DRDY) is used in analysis of the timing reference inherently through the resynchronization of the serial interface. The Applicant respectfully disagrees. Sanchez teaches a bi-directional synchronous serial interface. The controller is able to either write data to the peripheral or read data from the peripheral. Sanchez states:

> The peripheral receives and responds to the commands which consist of read or write operations. In a write operation the peripheral would wait for the data following the command word to be received on the SDI pin as shown in FIG. 3A. In a read operation, the peripheral 12 would provide data requested by the command word via the SDO pin, data availability being indicated by the DRDY pin as shown in FIG. 3B.

(Col. 4, lines 24-31).

In other words, the DRDY pin is only used during a read operation. DRDY is not asserted during write operations or during resynchronization of the controller and peripheral. Sanchez further states:

> The resynchronization method includes transmitting a sequence of a predetermined bit pattern from a controller wherein the pattern sequence is long enough that the peripheral will decode at least a portion of the sequence of serial data as a command word. The peripheral is reset upon receipt of a command word which has this predetermined logic pattern. The controller then transmits one bit opposite to the logic state of the next bit in

the pattern which indicates the alignment and causes the peripheral to come out of reset. Now the peripheral and controller are resynchronized in regards to the location of word boundaries and normal operation can continue.

(Col. 2, lines 54-65).

In other words, resynchronization is similar to a write operation, except the controller sends a predetermined bit pattern sequence to the peripheral, followed by a bit of the opposite logic. At no point does the peripheral send any data back. Since the peripheral does not transmit data back to the controller, DRDY is not used, and is not compared to the clock signal as part of the analysis of the timing reference.

Thus, the Applicant respectfully traverses the rejections to allowable independent claims 1, 14, and 27, and claims 3-9 and 16-22, which ultimately depend from allowable independent claims 1 and 14 respectively.

Claim Rejections Under 35 U.S.C. §103(a)

Claims 10-13, 23-26, and 30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sanchez and further in view of Sarangi et al. As claims 10-13, 23-26, and 30 depend from allowable independent claims 1, 14, and 27, they are not unpatentable over Sanchez for at least these reasons.

Also, Sarangi et al. and the present application are both assigned to the same entity, Intel Corporation. Accordingly, under 35 U.S.C. §103(c), the Sarangi reference cannot be used as a reference under 35 U.S.C. §103(a) because it is a 35 U.S.C. §102(e)-type reference.

In view of the amendments and remarks above, reconsideration and withdrawal of the rejection of claims 1-30 under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) are respectfully requested.

It is believed that this Amendment places the application in condition for allowance, and early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at (408) 975-7500.

The Office is hereby authorized to charge any fees, or credit any overpayments, to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON

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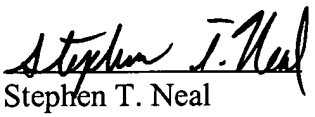
By: 
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